PATENT
S/N 09/747,901

Docket No. :1232-4667

Amendments to the Specification:

Please replace the paragraph beginning at page 29, line 16 through page 30, line 11 with the following amended paragraph:

> In the second line formed by R, G, and B data, R data are written in blocks 1, 4, and 7 in this order, G data are written in blocks 2, 5, and 8 in this order, and B data are written in blocks 3, 6, and 9 in this order. Before data are overwritten by this write operation, read is made from the first pixel of the previous line (i.e., the first line). That is, before R data are overwritten in blocks 1, 4, and 7 in this order, R, G, and B data of the first line are respectively read out from these blocks, and are supplied to the RGB/CMYK conversion circuit 211 via the sub-scan interpolation processor 209. Also, before G data are overwritten on blocks 2, 5, and 8 in this order, R, ~~G~~B, and B data of the first line are read out from these blocks and are supplied to the RGB/CMYK conversion circuit 211 via the sub-scan interpolation processor 209. Furthermore, before B data are overwritten on blocks 3, 6, and 9 in this order, R, ~~G~~B, and B data of the first line are read out from these blocks and are supplied to the RGB/CMYK conversion circuit 211 via the sub-scan interpolation processor 209.

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